

# Bulk Synthesis of Crystalline and Crystalline Core/Amorphous Shell Silicon Nanowires and Their Application for Energy Storage

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Silicon micro- and nanostructures have captivated much attention since 1964 due to the interest in studying the effect of diminution of size and dimension on its physical properties.<sup>1–5</sup> Silicon nanowire has been exploited for its application as a building block in bottom-up nanoelectronics,<sup>6,7</sup> photovoltaics,<sup>8–10</sup> biosensors,<sup>11</sup> and energy storage devices.<sup>12</sup> Having the ability to synthesize high-quality and a large quantity of Si nanowires is an important factor in the process to investigate the electrical, optical, and electrochemical properties of the material and in realization of the aforementioned applications. In many of the studies, crystalline and crystalline core/amorphous shell (c-core/a-shell) Si nanowires were synthesized *via* the vapor–liquid–solid (VLS) mechanism,<sup>1,13</sup> however, very often in small quantity. Si nanowires have been synthesized on many different substrates. For instance, vertically grown Si whiskers were synthesized on the Si(111) wafer first reported by Wagner, and he conducted a thorough fundamental study on the growth mechanism of this nanomaterial.<sup>1</sup> Cui *et al.* conducted an investigation of the relationship between the size of the catalyst and the diameter of the resulting Si nanowires on Si/SiO<sub>2</sub> wafers.<sup>4</sup> Chan *et al.* underwent the study of the electrochemical properties of Si nanowires on stainless steel as an anode material for Li-ion batteries.<sup>12</sup> These syntheses can be defined as growth on two-dimensional (2-D) planar substrates, and often a relatively small quantity of nanowires is grown with this method. The ability to synthesize bulk quantities of Si nanowires is advantageous in many of the aforementioned applications. Different mechanisms for achieving

**ABSTRACT** Silicon nanowires (NWs) have stimulated significant interest and found numerous applications; however, many applications will require a bulk quantity of nanowires to be synthesized in a reliable way. In this paper, we report the bulk synthesis of silicon nanowires on millimeter scale Al<sub>2</sub>O<sub>3</sub> spheres with a thermal chemical vapor deposition system (CVD) *via* the vapor–liquid–solid (VLS) growth mechanism. The spherical substrates enable the realization of Si nanowire synthesis on three-dimensional surfaces in comparison with the synthesis on a planar, two-dimensional wafer substrate. By modifying temperature in the recipe of synthesis, both single-crystalline and crystalline core/amorphous shell Si nanowires were obtained with this nanowire-on-spherical-support method. Conspicuous distinction in crystallinity of the nanowires was revealed by transmission electron microscopy characterization. The crystalline core/amorphous shell Si nanowires were utilized to form the anode of Li-ion battery half-cells with the traditional slurry method. Galvanostatic measurement demonstrated that the maximum power capacity achievable by the electrodes was 3500 mAh/g and capacity sustained at 1100 mAh/g after 60 cycles of charging and discharging.

**KEYWORDS:** silicon nanowires · spheres · bulk synthesis · three-dimensional synthesis · Li-ion battery · crystalline core/amorphous shell

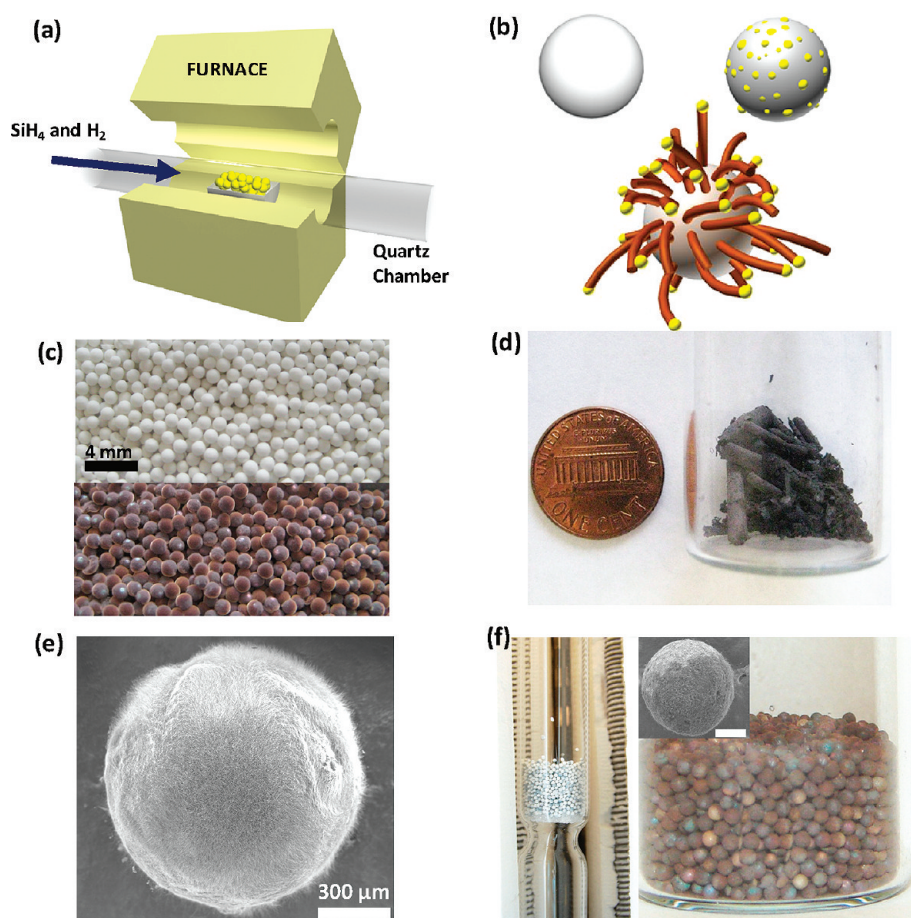
growth of bulk quantities of nanowires have been actively studied.<sup>5,14–18</sup> In particular, Wang *et al.* explored the concept of the synthesis of a high quantity of germanium nanowires on irregular silica particles. In his experiments, he had proven that a higher quantity of nanowires can be produced by replacing the 2-D substrates with three-dimensional (3-D) substrates.<sup>16,17</sup> One of the many important applications of Si nanowires in bulk quantity is the study of expending Si nanowires as the active material in the anode of Li-ion batteries. In a traditional slurry electrode fabrication process, which is used for commercialized batteries, a current collector is coated with a layer of slurry of amalgamation formed by active materials, composite of ionic conduction, and binder.<sup>19</sup> Tens of milligrams of the active material are required in the processing of traditional slurry electrodes.

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**Figure 1.** (a) Schematic diagram illustrating a nanowire synthesis system composed of a furnace and a quartz reaction chamber. A quartz boat loaded with Au-coated  $\text{Al}_2\text{O}_3$  spheres was placed at the center of the chamber. (b) Schematic diagram showing a pristine  $\text{Al}_2\text{O}_3$  sphere, an  $\text{Al}_2\text{O}_3$  sphere decorated with Au particles after annealing, and Si nanowires synthesized on  $\text{Al}_2\text{O}_3$  spheres *via* the VLS mechanism. (c) Photographic image of  $\text{Al}_2\text{O}_3$  spheres before (top) and after (bottom) nanowire synthesis. (d) Photographic image of 80 mg of free-standing silicon nanowires in a vial. (e) SEM image of crystalline core/amorphous shell Si nanowires synthesized on a millimeter scale  $\text{Al}_2\text{O}_3$  sphere. (f)  $\text{Al}_2\text{O}_3$  spheres stacked in a vertical quartz reaction chamber (left). Photographic image and SEM image (inset) of  $\text{Al}_2\text{O}_3$  spheres with Si nanowires synthesized with the vertical chamber configuration (right). The scale bar is 400  $\mu\text{m}$ .

Synthesis of silicon nanowires in bulk quantity can enable the material to be adopted in the commercially compatible slurry electrode fabrication process.

In this paper, we report a scalable methodology for synthesis of Si nanowires *via* the vapor–liquid–solid (VLS) mechanism. The nanowires were synthesized three-dimensionally (3-D) on aluminum oxide ( $\text{Al}_2\text{O}_3$ ) millimeter spheres decorated with gold (Au) nanoclusters. Both single-crystalline and crystalline core/amorphous shell (c-core/a-shell) Si nanowires were obtained with this method by varying the growth recipe. The crystallography of the nanowires was characterized by high-resolution transmission electron microscopy (HRTEM) and electron diffraction patterns. The c-core/a-shell Si nanowires were utilized as the active anode material in Li-ion battery half-cells to demonstrate an application of the Si nanowires grown with this scalable method. The specific capacity of the half-cells was sustained at 1100 mAh/g after 60 cycles as measured in the galvanostatic charge–discharge experiment.

## RESULTS AND DISCUSSION

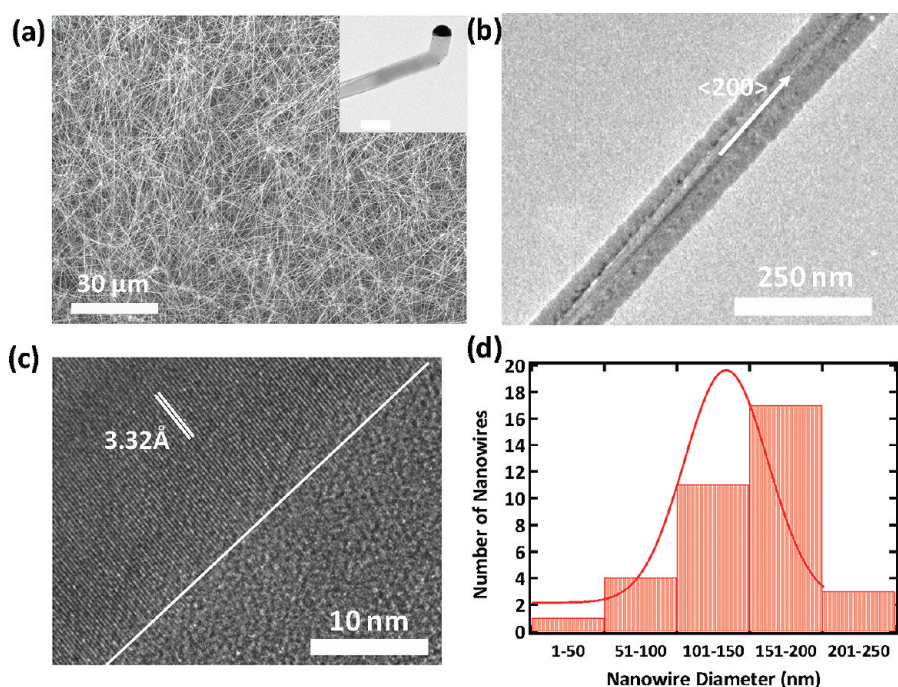
In order to achieve synthesis of Si nanowires in a scalable manner,  $\text{Al}_2\text{O}_3$  spheres with diameters ranging from 0.79 to 1.18 mm (GlenMills, Inc.) were used as the supporting substrate for the synthesis. In this study, the Si nanowires were synthesized in a low-pressure chemical vapor deposition (LPCVD) system, as illustrated in Figure 1a. To form the catalytic Au nanoclusters for the growth, Au film of 2 nm was deposited on the surface of the spheres by e-beam evaporation. Thermal annealing of the sphere covered in Au film was performed at 530 °C under 20 Torr of pressure with constant flow of 100 sccm of  $\text{H}_2$  for 30 min. At elevated temperature, Au nanoclusters were formed during the annealing process, as shown in Figure 1b. Our method works as a simple and reliable way to achieve gold nanoclusters with narrow diameter distribution, which is sufficient for producing silicon nanowires for certain applications such as an anode for a Li-ion battery. The  $\text{Al}_2\text{O}_3$  spheres decorated with Au nanoclusters were

contained in a quartz boat, and it was loaded and positioned at the center of a horizontally oriented quartz growth chamber inside the furnace, as shown in Figure 1a. During the synthesis, the temperature of the growth chamber was increased to 450–530 °C depending on the requirement of crystallinity on the resulting nanowires. The pressure in the chamber was controlled at 100 Torr while supplying a constant flow of silane ( $\text{SiH}_4$ , 2% silane in argon) and hydrogen ( $\text{H}_2$ , ultrahigh-purity hydrogen) at 111 and 20 sccm, respectively. The Au nanoclusters served as catalytic sites for Si nucleation during the VLS process of the synthesis. The diameter of the nanoclusters is proportional to the thickness of the Au film and varies within a certain range. More accurate control over the nanocluster and resulting nanowire diameter can be obtained by deposition of presynthesized gold nanoclusters of desired diameters onto the spherical substrates<sup>20</sup> or by using the aqueous impregnation method<sup>21</sup> or surface functionalization of the substrates.<sup>16</sup>

Si nanowires have been reported to be synthesized via the VLS mechanism in various substrates including Si wafers,<sup>2</sup> Si/SiO<sub>2</sub> wafers,<sup>4</sup> and stainless steel foil.<sup>12,13</sup> In all of these reports, the nanowires were synthesized on a two-dimensional planar substrate. Three-dimensional growth substrates had been proven to contribute to the higher quantity of nanowire synthesis due to their large surface areas.<sup>16,17</sup> In order to achieve bulk synthesis of Si nanowires, we conducted studies of silicon nanowire growth on a 3-D substrate, namely, on Al<sub>2</sub>O<sub>3</sub> spheres. The spherical Al<sub>2</sub>O<sub>3</sub> substrates provided a large surface area for the nanowire growth, hence resulting in high nanowire quantity. To the best of our knowledge, this is the first report of Si nanowires synthesized on Al<sub>2</sub>O<sub>3</sub> spheres via the VLS mechanism. The surface of the liquid Au–Si alloy droplets formed during the VLS growth process has a large accommodation coefficient, which gives rise to the preferential deposition of Si atoms onto the liquid droplet as explained by Wagner.<sup>2</sup> The advantageous characteristic allows Si nanowires to be synthesized on any substrate, hence allowing the Al<sub>2</sub>O<sub>3</sub> sphere to be a valid choice for the growth substrate of the synthesis. The two photographic images in Figure 1c show the difference in the external appearance of the Al<sub>2</sub>O<sub>3</sub> spheres before and after the synthesis. There is an apparent change in the color of the spheres, from white to brown. A typical SEM image of Si nanowires synthesized on a single Al<sub>2</sub>O<sub>3</sub> sphere is illustrated in Figure 1e. The sphere is clearly covered with a high density of nanowires grown in random directions, which demonstrates the validity of three-dimensional synthesis. Nanowires were not only grown on Al<sub>2</sub>O<sub>3</sub> spheres situated on the surface of the sphere stack but also can be observed on the surface of the spheres buried underneath. Due to the large diameter of spheres, the precursor ( $\text{SiH}_4$ ) can diffuse through the

interstices between the spheres situated on the surface and can reach the buried spheres during the synthesis.<sup>22</sup> The property mentioned above can enable the spheres to be stacked in multiple layers, results in enhancement of loading during each round of the synthesis, and gives rise to synthesis of Si nanowires in bulk quantity. The Si nanowires can be easily removed from the surface of the spheres by applying ultrasonication on spheres in solvent (*i.e.*, isopropyl alcohol) or by simply exerting vibration on the spheres in solvent. In order to extract nanowires from the solution, the solution was dispersed onto a piece of a microscope slide, and at elevated temperature (80 °C), the solvent was evaporated, leaving behind a layer of nanowire film. After removing the nanowire film from the microscope slide, the nanowires appeared as black materials being contained in a glass vial, and the total weight of the nanowires in the vial was 80 mg, as depicted in Figure 1d. To further increase the yield of the synthesis method, the growth chamber along with the furnace can be oriented in the vertical direction, as demonstrated in Figure 1f. The aforementioned configuration of the growth chamber enables a higher quantity of Al<sub>2</sub>O<sub>3</sub> spheres to be loaded, hence leading to a higher yield of the Si nanowires. Photographic images of the Al<sub>2</sub>O<sub>3</sub> spheres before and after synthesis are shown in Figure 1f. The SEM image of an Al<sub>2</sub>O<sub>3</sub> sphere with as-grown Si nanowires in the inset of Figure 1f demonstrates the validity of the scheme.

Both single-crystalline and crystalline core/amorphous shell Si nanowires were successfully synthesized by the nanowire-on-sphere methodology. The two types of Si nanowires have been found in applications reported in literature including energy storage devices,<sup>12</sup> transistors,<sup>6</sup> and photovoltaics.<sup>10,23</sup> Having the ability to produce both single-crystalline and c-core/a-shell Si nanowires in bulk quantity provides a source for scaling up the aforementioned nanowire-related applications, and one example is the anode for a Li-ion battery. Figure 2a shows a typical SEM image of the as-grown crystalline core/amorphous shell Si nanowires on Al<sub>2</sub>O<sub>3</sub> spheres, which were synthesized under a constant flow rate of  $\text{SiH}_4$  and  $\text{H}_2$  at 111 and 20 sccm, respectively. The growth temperature was elevated to 530 °C and was under 100 Torr of pressure (detailed description of the synthesis can be found in the Methods section). The nanowires are between 40 and 100  $\mu\text{m}$  in length, and the density is approximately 6 nanowires per  $\mu\text{m}^2$  (NWs/ $\mu\text{m}^2$ ). From the inset of Figure 2a, a Au particle can be clearly observed on the tip of a single nanowire, giving evidence to the fact that the nanowire growth was based on the VLS mechanism. Figure 2b is a typical TEM image showing the core/shell morphology of the nanowire. The clear contrast reveals the conspicuous boundary between the core and the shell. To illustrate the c-core/a-shell structure of the nanowires, a high-resolution transmission electron microscopic (HRTEM)

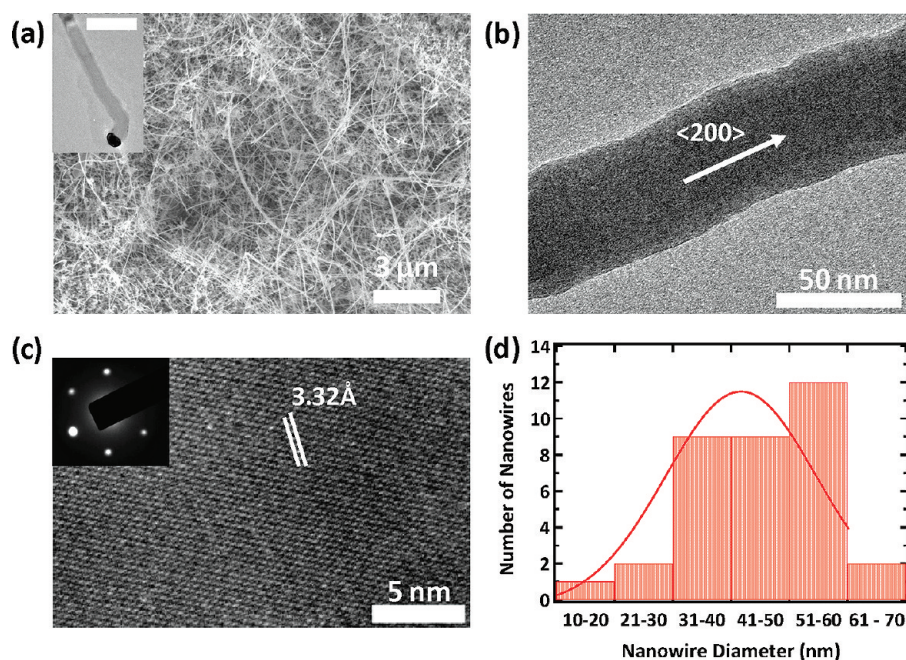


**Figure 2.** (a) FESEM image of crystalline core/amorphous shell Si nanowires grown on an  $\text{Al}_2\text{O}_3$  sphere. Inset: SEM image of a c-core/a-shell Si nanowire with a Au catalytic particle at its tip. Scale bar is 100 nm. (b) TEM image of a c-core/a-shell Si nanowire. (c) HRTEM image of crystalline core/amorphous shell interface of a Si nanowire. (d) Diameter distribution of the c-core/a-shell Si nanowires.

image is presented in Figure 2c. The periodic planes in the crystalline core give rise to constructive interference of the deflected electron waves in the TEM and resulting in lattice fringes, as shown in the figure. There is a clear boundary between the fringes resulting from crystalline lattice of the core and the amorphous shell of the Si nanowire in Figure 2c. The spacing between contiguous planes in the Si nanowire was measured to be 3.32 Å based on the lattice fringe depicted in Figure 2c. The plane spacing corresponds to the  $\langle 200 \rangle$  direction as the preferential growth direction of the nanowire. The majority of the nanowires synthesized at the aforementioned growth condition exhibit diameters ranging between 151 and 200 nm, as illustrated in Figure 2d. A Gaussian fit of nanowire diameter distribution yields a mean value of 149 nm and a standard deviation value of 40 nm. The variation in diameter of the nanowires can be ascribed to the property of lateral diffusion of the Au droplets during the annealing process and during the growth.<sup>24</sup> Study has shown that the Au droplet might migrate during the growth from smaller Au droplets to large ones, hence resulting in variation of diameter of the nanowires.<sup>24</sup> The amorphous shell of the nanowires can be attributed to the simultaneous deposition of Si via the vapor–solid (VS) mechanism during the growth.<sup>25</sup> The VS deposition increases with temperature, and later in this paper, it will be shown that the amorphous layer can be eliminated by conducting the synthesis at a lower temperature. The crystalline core/amorphous shell silicon nanowires can be a highly

desirable candidate working as the active anode material in Li-ion batteries, as reported previously by Cui *et al.*<sup>13</sup>

Single-crystalline Si nanowires had also been synthesized on the  $\text{Al}_2\text{O}_3$  spheres with a similar reaction recipe. The process of the synthesis was almost the same as the procedure mentioned in the previous section of this paper except for the growth temperature, which was controlled at 455 °C in order to attain the single-crystalline nanowires (detail description of the synthesis can be found in the Methods section). The volume of the Si–Au alloy can be controlled by the temperature during the VLS process,<sup>25</sup> and Westwater illustrated that Si nanowires with a smaller diameter can be obtained at lower temperature than that at higher temperature.<sup>3</sup> An SEM image of the as-grown nanowires on a sphere is shown in Figure 3a. The average length of the nanowires is estimated to be 10 μm, as shown in the figure, which is at least 4 times shorter than that of the crystalline core/amorphous shell nanowires. The density of the nanowires is approximately 10 NWs/μm<sup>2</sup>. The inset in Figure 3a shows the Au particle tip formed at one end of a Si nanowire, and that reveals that the nature of the growth was based on the VLS mechanism. A typical TEM image of the Si nanowire is illustrated in Figure 3b. The diameter of the nanowire is 48 nm in the image, which is 3 times smaller than the diameter of the c-core/a-shell Si nanowires. The spacing between contiguous planes in the Si nanowire was measured to be 3.32 Å based on the lattice fringe illustrated in Figure 3c. The plane



**Figure 3.** (a) FESEM image of single-crystalline Si nanowires grown on an  $\text{Al}_2\text{O}_3$  sphere. Inset: crystalline silicon nanowire with an Au particle at its tip. The scale bar is 100 nm. (b) TEM image of a single-crystalline Si nanowire having the growth axis in the  $\langle 111 \rangle$  direction. (c) HRTEM image showing the lattice fringes of the nanowire. Inset: electron diffraction pattern from the silicon nanowire. (d) Diameter distribution of the single-crystalline nanowires.

spacing corresponds to the  $\langle 200 \rangle$  direction as the preferential growth direction of the nanowire. The diameter of the nanowires synthesized under the aforementioned condition varies from 10 to 70 nm, with the majority of the diameter of the nanowires between 30 and 60 nm, as illustrated in Figure 3d. A Gaussian fit of nanowire diameter distribution yields a mean value of 44 nm and a standard deviation value of 11 nm. As it was shown by the results, crystalline Si nanowires can be synthesized on the  $\text{Al}_2\text{O}_3$  spheres by varying the growth temperature in the reaction chamber. These crystalline nanowires with smaller diameter can be used to study their electronic transport properties. The electrical properties of the Si nanowires can be improved by incorporating n-type or p-type dopant atoms into the nanowires with this scheme. Gaseous phase dopants, such as phosphine ( $\text{PH}_3$ ) or diborane ( $\text{B}_2\text{H}_6$ ), can be introduced into the reaction chamber during the synthesis to achieve doping of the nanowires.<sup>6,26</sup>

As it was mentioned in the earlier part of this report, crystalline core/amorphous shell Si NWs have been demonstrated to be a desirable anode material for Li-ion batteries.<sup>13</sup> In order to demonstrate one of the many applications of our Si nanowires obtained by the bulk synthesis scheme, we conducted a series of studies in the electrochemical properties of the crystalline core/amorphous shell Si nanowires. The c-core/a-shell Si nanowires were mixed with ion conducting composite and binder to form a layer of uniform slurry. Anode is formed by dispersion of the slurry on a copper sheet, as the current collecting layer. The anode is assembled into a coin cell in conjunction with

electrolyte and lithium counter electrode (detailed description of the fabrication process can be found in the Methods section). The nanowires were utilized as active materials in the electrode of electrochemical cells. The cyclic voltammetry (CV) profile of the Si nanowire electrodes was obtained by a potentiostat (Gamry, Reference 600) using a potential window of 0.01 to 3.0 V for three cycles. The result of the CV measurement is depicted in Figure 4a with scan rate of 0.05 mV/s. When the potential was incremented from 3.0 to 0.01 V during the first discharging cycles, the Si nanowires exhibited typical crystalline core/amorphous shell features. First, there is an apparent peak at around 250 mV due to lithiation of the amorphous Si shell, which agreed with the previous thin film study conducted by Maranchi *et al.*<sup>27</sup> Second, the small peak near 130 mV is attributed to the amorphization of crystalline Si during the first lithiation process.<sup>12,28</sup> Furthermore, further discharging results in the formation of a new phase,  $\text{Li}_{15}\text{Si}_4$ , from the amorphous Li-Si alloy at the peak potential around 55 mV, which was suggested by a previous study on Si powder and films.<sup>29</sup> Upon the charging process, the peak at 390 mV indicates a transformation by means of the coexistence of two phases of both crystalline and amorphous Li-Si alloy.<sup>29</sup> After the first cycle of discharge and charge between 3.0 and 0.01 V, the peak for crystalline Si was drastically diminished, demonstrating that the crystalline core/amorphous shell structure was completely transformed into the amorphous phase. The second and the third cycles match relatively well, which implies that the system had reached a steady state.

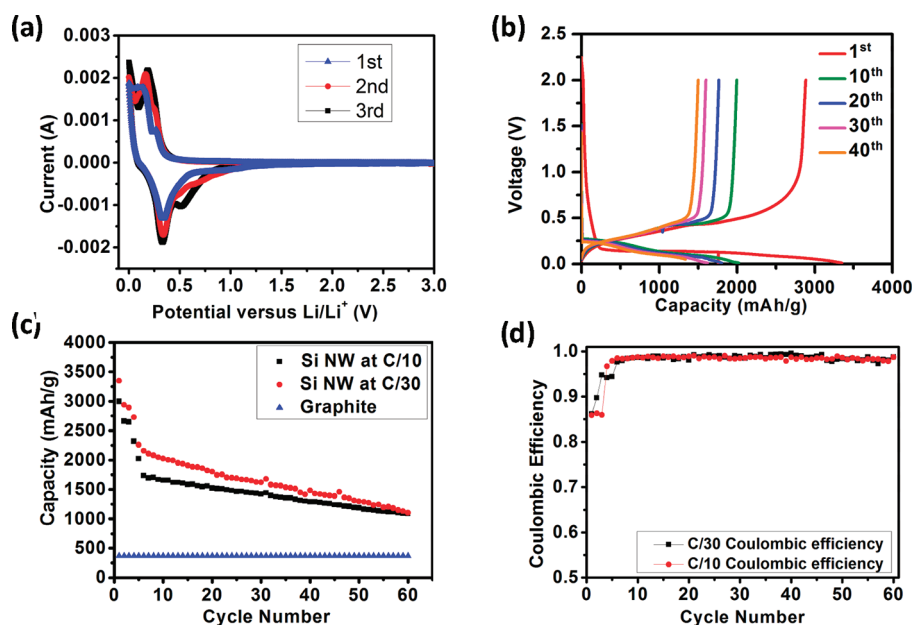


Figure 4. (a) Cyclic voltammogram for Si nanowires from 0.01 to 3.0 V. The first three cycles are shown. (b) Voltage profile for the first 40 cycles of the Si nanowire electrode at the C/30 rate. (c) Capacity versus cycle number for the Si nanowire electrode at the C/30 (red) rate and the C/10 (black) rate. (d) Coulombic efficiency versus cycle number for the Si nanowire electrode at the C/30 (red) rate and the C/10 (black) rate.

Figure 4b,c illustrates the galvanostatic (GV) charging and discharging measurements, carried out by a battery testing system (MSTAT, Arbin), determining the specific capacity ( $C_{sp}$ ) and the Coulombic efficiency of the devices in a two-electrode configuration. Computation of different current rates was based on the capacity in the first discharging process. Figure 4b is the charging–discharging performance of the Si nanowire electrodes for 40 cycles with a current rate of C/30. The slow cycling current reveals much electrochemical information related to the electrode structure. In the initial state, the potential dropped to 200 mV and was maintained at a prolonged flat plateau at around 100 mV, then gradually decreased to zero. This plateau resulted from the coexistence of partially lithiated amorphous Si shell accompanied by amorphization of a crystalline Si core. The capacity in the first discharging cycle reached up to 3500 mAh/g, very close to the theoretical capacity of silicon.<sup>30</sup> For the following cycles, the plateau is stable at 240 mV, which is consistent with the conclusion from Figure 4a, that after the first cycle, almost all of the crystalline core/amorphous shell nanowires had transformed into the amorphous phase. Furthermore, we can still observe the small plateau at about 50 mV because of the emergence of the new phase, which was also explained in the earlier discussion for Figure 4a.

To further investigate the GV behavior of the Si nanowires from bulk synthesis, we cycled the electrode with two different current rates, C/30 and C/10. The relationship between discharging specific capacity and cycle number is illustrated in Figure 4c. As it can be observed in the figure, the Si nanowire electrodes

display relatively high capacity value at both current rates for 60 cycles, which are more than two factors of the specific capacity value exhibited by the commercially available graphite anodes. The high specific capacity can be attributed to the small dimension of the nanowires, which enables better ion accommodation, and the one-dimensional electronic pathway gives rise to improved charge transport. The Si nanowire electrode exhibits relatively small irreversible capacity of 10%. The retention of C/10 current rate is higher than that of the C/30 rate. That may be attributed to different degrees of Si involvement in the lithiation/delithiation process. For C/30, the small current allows the electrode materials to react more thoroughly; therefore, more Si nanowires can participate in lithiation, resulting in higher specific capacity but at the same time larger volume expansion. The large volume expansion could damage the intact electrode structure, thereby having a negative effect on capacity retention.

Moreover, the Coulombic efficiency of our devices was calculated and plotted in Figure 4d, which further demonstrates the excellent battery performance of the Si nanowires obtained from the bulk synthesis method. In the second cycle, the efficiency at both the C/30 and C/10 current rate was increased to 90%, and in the cycles following that, the efficiency was sustained at around 98–99%. The efficiency is comparable to the efficiency of the anodes in commercial Li-ion batteries. The only difference in Coulombic efficiency for the two current rates is that the charging–discharging experiment conducted under the higher current rate required a few additional cycles to reach 99% Coulombic efficiency value. That is caused by the fact that, with

larger current, more cycles of repeated lithiation are required to transform all crystalline core/amorphous shell structures into the amorphous phase.

By now, the bulk synthesis of silicon nanowires and their application for Li-ion batteries has been elucidated. We note that our bulk synthesis approach can be applied to produce many other nanowire materials, for instance, indium oxide NWs,<sup>31</sup> tin oxide NWs,<sup>32</sup> zinc oxide NWs,<sup>33,34</sup> gallium nitride NWs,<sup>20</sup> Ge/Si core-shell nanowires<sup>35</sup> via LPCVD, and III–V nanowires with MOCVD.<sup>36</sup> These nanowires can be expended for a wide variety of applications that may require bulk quantity, for instance, nanowires in thin film transistors for display applications<sup>37,38</sup> and electronic skins.<sup>39</sup> We further note that bulk synthesis of nanowires can also be potentially achieved by utilization of other techniques such as fluidized-bed synthesis,<sup>40</sup> which is currently being investigated in our group.

## METHODS

**Synthesis of Crystalline Core/Amorphous Shell Si Nanowires and Single-Crystalline Si Nanowires.** For synthesis of crystalline core/amorphous shell Si nanowires, the millimeter scale Al<sub>2</sub>O<sub>3</sub> spheres decorated with Au nanoclusters were placed in a quartz boat, which was placed at the center of a growth chamber inside a horizontal tube furnace. The chamber was evacuated to 20 Torr and was purged with ultrahigh-purity hydrogen gas for 10 min to remove oxygen in the chamber. The temperature of the chamber was increased from room temperature to 530 °C in 10 min. At 530 °C, SiH<sub>4</sub> was introduced into the chamber at 111 sccm and the H<sub>2</sub> flow rate was controlled at 20 sccm. The pressure inside the chamber was maintained at approximately 100 Torr during the growth, and the growth time was 25 min. At the end of the growth, SiH<sub>4</sub> gas was turned off and the flow rate of H<sub>2</sub> was adjusted to 100 sccm, while the chamber was cooled to room temperature. The procedure for the synthesis of single-crystalline Si nanowires is almost the same as the one for synthesis of crystalline core/amorphous shell nanowires, except the growth temperature was maintained at 455 °C.

**Fabrication of Si Nanowire Anodes.** The electrodes were made by mixing the Si nanowires with SuperP conductive carbon black and sodium carboxymethylcellulose (CMC) (MW 90 000, Aldrich) in water (10 wt %) to form a uniform slurry and then spread onto a copper foil using a stainless steel blade. The electrode was dried at 50 °C overnight in air and was maintained at room temperature in Ar for 2 h just prior to cell assembly to remove any residual water vapor. The loading density of our Si nanowires was estimated to be 1 mg/cm<sup>2</sup>. Then CR2032 coin cells were assembled in an Ar-filled glovebox using the as-prepared Si nanowire anodes as working electrodes and lithium metal foil as counter electrodes. The electrolyte was 1 M LiClO<sub>4</sub> dissolved in a 1:1 (weight ration) mixture of ethylene carbonate (EC) and diethyl carbonate (DEC).

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## REFERENCES AND NOTES

- Wagner, R. S.; Ellis, W. C. Vapor–Liquid–Solid Mechanism of Single Crystal Growth. *Appl. Phys. Lett.* **1964**, *4*, 89.
- Wagner, R. S.; Ellis, W. C. The Vapor–Liquid–Solid Mechanism of Crystal Growth. *J. Vac. Sci. Technol.* **1965**, *233*, 1054.
- Westwater, J.; Gosain, D. P.; Tomiya, S.; Usui, S.; Ruda, H. Growth of Silicon Nanowires via Gold/Silane Vapor–

Liquid–Solid Reaction. *J. Vac. Sci. Technol., B* **1997**, *15*, 554–557.

- Cui, Y.; Lauhon, L. J.; Gudiksen, M. S.; Wang, J.; Lieber, C. M. Diameter-Controlled Synthesis of Single-Crystal Silicon Nanowires. *Appl. Phys. Lett.* **2001**, *78*, 2214.
- Morales, A. M.; Lieber, C. M. A Laser Ablation Method for the Synthesis of Crystalline Semiconductor Nanowires. *Science* **1998**, *279*, 208.
- Cui, Y.; Lieber, C. M. Functional Nanoscale Electronic Devices Assembled Using Silicon Nanowire Building Blocks. *Science* **2001**, *291*, 851.
- Cui, Y.; Zhong, Z.; Wang, W. U.; Lieber, C. M. High Performance Silicon Nanowire Field Effect Transistors. *Nano Lett.* **2003**, *3*, 149–152.
- Hu, L.; Chen, G. Analysis of Optical Absorption in Silicon Nanowire Arrays for Photovoltaic Applications. *Nano Lett.* **2007**, *7*, 3249.
- Boettcher, S. W.; Spurgeon, J. M.; Putnam, M. C.; Warren, E. L.; Turner-Evans, D. B.; Kelzenberg, M. D.; Maiolo, J. R.; Atwater, H. A.; Lewis, N. S. Energy-Conversion Properties of Vapor–Liquid–Solid-Grown Silicon Wire-Array Photocathodes. *Science* **2010**, *327*, 185–187.
- Putnam, M. C.; Boettcher, S. W.; Kelzenberg, M. D.; Turner-Evans, D. B.; Spurgeon, J. M.; Warren, E. L.; Briggs, R. M.; Lewis, N. S.; Atwater, H. A. Si Nanowire-Array Solar Cells. *Energy Environ. Sci.* **2010**, *3*, 1037–1041.
- Cui, Y.; Wei, Q.; Park, H.; Lieber, C. M. Nanowire Nanosensors for Highly Sensitive and Selective Detection of Biological and Chemical Species. *Science* **2001**, *293*, 1289.
- Chan, C. K.; Peng, H.; Liu, G.; McIlwrath, K.; Zhang, X. F.; Huggins, R. A.; Cui, Y. High-Performance Lithium Battery Anodes Using Silicon Nanowires. *Nat. Nanotechnol.* **2008**, *3*, 31.
- Cui, L.-F.; Ruffo, R.; Chan, C. K.; Peng, H.; Cui, Y. Crystalline–Amorphous Core–Shell Silicon Nanowires for High Capacity and High Current Battery Electrodes. *Nano Lett.* **2009**, *9*, 491–495.
- Holmes, J. D.; Johnston, K. P.; Doty, R. C.; Korgel, B. A. Control of Thickness and Orientation of Solution-Grown Silicon Nanowires. *Science* **2000**, *287*, 1471–1473.
- Greene, L. E.; Law, M.; Goldberger, J.; Kim, F.; Johnson, J. C.; Zhang, Y.; Saykally, R. J.; Yang, P. Low-Temperature Wafer-Scale Production of ZnO Nanowire Arrays. *Angew. Chem., Int. Ed.* **2003**, *42*, 3031–3034.
- Wang, D.; Chang, Y.-L.; Liu, Z.; Dai, H. Oxidation Resistant Germanium Nanowires: Bulk Synthesis, Long Chain Alkanethiol Functionalization, and Langmuir–Blodgett Assembly. *J. Am. Chem. Soc.* **2005**, *127*, 11871–11875.

17. Wang, D.; Dai, H. Germanium Nanowires: From Synthesis, Surface Chemistry, and Assembly to Devices. *Appl. Phys. A: Mater. Sci. Process.* **2006**, *85*, 217–225.
18. Pan, Z. W.; Dai, Z. R.; Wang, Z. L. Nanobelts of Semiconducting Oxides. *Science* **2001**, *291*, 1947–1949.
19. Chan, C. K.; Patel, R. N.; O'Connell, M. J.; Korgel, B. A.; Cui, Y. Solution-Grown Silicon Nanowires for Lithium-Ion Battery Anodes. *ACS Nano* **2010**, *4*, 1443–1450.
20. Han, S.; Jin, W.; Tang, T.; Li, C.; Zhang, D.; Liu, X.; Han, J.; Zhou, C. Controlled Growth of Gallium Nitride Single-Crystal Nanowires Using a Chemical Vapor Deposition Method. *J. Mater. Res.* **2003**, *18*, 245–249.
21. Xu, Q.; Kharas, K. C. C.; Datye, A. K. The Preparation of Highly Dispersed Au/Al<sub>2</sub>O<sub>3</sub> by Aqueous Impregnation. *Catal. Lett.* **2003**, *85*, 229–235.
22. Xiang, R.; Luo, G.; Qian, W.; Wang, Y.; Wei, F.; Li, Q. Large Area Growth of Aligned CNT Arrays on Spheres: Towards Large Scale and Continuous Production. *Chem. Vap. Deposition* **2007**, *13*, 533–536.
23. Kelzenberg, M. D.; Boettcher, S. W.; Petykiewicz, J. A.; Turner-Evans, D. B.; Putnam, M. C.; Warren, E. L.; Spurgeon, J. M.; Briggs, R. M.; Lewis, N. S.; Atwater, H. A. Enhanced Absorption and Carrier Collection in Si Wire Arrays for Photovoltaic Applications. *Nat. Mater.* **2010**, *9*, 239.
24. Hannon, J. B.; Kodambaka, S.; Ross, F. M.; Tromp, R. M. The Influence of the Surface Migration of Gold on the Growth of Silicon Nanowires. *Nature* **2006**, *440*, 69.
25. Wagner, R. S.; Doherty, C. J. Controlled Vapor–Liquid–Solid Growth of Silicon Crystals. *J. Electrochem. Soc.* **1966**, *113*, 1300.
26. Cui, Y.; Duan, X.; Hu, J.; Lieber, C. M. Doping and Electrical Transport in Silicon Nanowires. *J. Phys. Chem. B* **2000**, *104*, 5213.
27. Maranchi, J. P.; Hepp, A. F.; Kumta, P. N. High Capacity, Reversible Silicon Thin-Film Anodes for Lithium-Ion Batteries. *Electrochem. Solid-State Lett.* **2003**, *6*, A198–A201.
28. Limthongkul, P.; Jang, Y.-I.; Dudney, N. J.; Chiang, Y.-M. Electrochemically-Driven Solid-State Amorphization in Lithium-Silicon Alloys and Implications for Lithium Storage. *Acta. Mater.* **2003**, *2003*, 1103–1113.
29. Obrovac, M. N.; Krause, L. J. Reversible Cycling of Crystalline Silicon Powder. *J. Electrochem. Soc.* **2007**, *154*, A103–A108.
30. Boukamp, B. A.; Lesh, G. C.; Huggins, R. A. All-Solid Lithium Electrodes with Mixed-Conductor Matrix. *J. Electrochem. Soc.* **1981**, *128*, 725–729.
31. Li, C.; Lei, B.; Zhang, D.; Liu, X.; Han, S.; Tang, T.; Rouhanizadeh, M.; Hsiai, T.; Zhou, C. Chemical Gating of In<sub>2</sub>O<sub>3</sub> Nanowires by Organic and Biomolecules. *Appl. Phys. Lett.* **2003**, *83*, 4014–4016.
32. Liu, Z.; Zhang, D.; Han, S.; Li, C.; Tang, T.; Jin, W.; Liu, X.; Lei, B.; Zhou, C. Laser Ablation Synthesis and Electron Transport Studies of Tin Oxide Nanowires. *Adv. Mater.* **2003**, *15*, 1754–1757.
33. Wang, Z. L.; Song, J. Piezoelectric Nanogenerators Based on Zinc Oxide Nanowire Arrays. *Science* **2006**, *312*, 242–246.
34. Huang, M. H.; Mao, S.; Feick, H.; Yan, H.; Wu, Y.; Kind, H.; Weber, E.; Russo, R.; Yang, P. Room-Temperature Ultraviolet Nanowire Nanolasers. *Science* **2001**, *292*, 1897–1899.
35. Lauthon, L. J.; Gudiksen, M. S.; Wang, D.; Lieber, C. M. Epitaxial Core–Shell and Core–Multishell Nanowire Heterostructures. *Nature* **2002**, *420*, 57–61.
36. Jhansson, J.; Karlsson, L. S.; Svensson, C. P. T.; Martensson, T.; Wacaser, B. A.; Deppert, K.; Samuelson, L.; Seifert, W. Structural Properties of <111> B-Oriented III–V Nanowires. *Nat. Mater.* **2006**, *5*, 574–580.
37. Ju, S.; Li, J.; Liu, J.; Chen, P.-C.; Ha, Y.-G.; Ishikawa, F.; Chang, H.; Zhou, C.; Facchetti, A.; Janes, D. B.; Marks, T. J. Transparent Active Matrix Organic Light-Emitting Diode Displays Driven by Nanowire Transistor Circuitry. *Nano Lett.* **2008**, *8*, 997–1004.
38. Chen, P.-C.; Shen, G.; Chen, H.; Ha, Y.-G.; Wu, C.; Sukcharoenchoke, S.; Fu, Y.; Liu, J.; facchetti, A.; Marks, T. J.; Thompson, M. E.; Zhou, C. High-Performance Single-Crystalline Arsenic-Doped Indium Oxide Nanowires for Transparent Thin-Film Transistors and Active Matrix Organic Light-Emitting Diode Displays. *ACS Nano* **2009**, *3*, 3383–3390.
39. Takei, K.; Takahashi, T.; Ho, J. C.; Ko, H.; Gillies, A. G.; Leu, P. W.; Fearing, R. S.; Javey, A. Nanowire Active-Matrix Circuitry for Low-Voltage Macroscale Artificial Skin. *Nat. Mater.* **2010**, *9*, 821–826.
40. Liu, Y.; Qian, W.; Zhang, Q.; Ning, G.; Luo, G.; Wang, Y.; Wang, D.; Wei, F. Synthesis of High-Quality, Doubled-Walled Carbon Nanotubes in Fluidized Bed Reactor. *Chem. Eng. Technol.* **2009**, *32*, 73–79.